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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,951	10/30/2001	Frederic Reblewski	109894-129745	4750

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EXAMINER	
PALADINI, ALBERT WILLIAM	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,951	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-16* is/are allowed.

6)☒ Claim(s) *17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/02,3/03,1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: None of the art searched or the references cited disclose or teach alone or in combination the emulation logic board containing the plurality of I/O pins, the plurality of integrated circuits with reconfigurable circuits, the on-board data processing resources coupled to the integrated circuits which generates a first configuration signal to configure selected reconfigurable logic resources, and the second configuration signal to configure selected reconfigurable interconnect recourses responsive to external requests.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski (6265894) in view of Reblewski (6473726).

In figure 10 Reblewski (6265894) discloses an emulation system 1000 comprising host system 1020 communicatively coupled to emulator 1060. Emulator 1060 includes emulation array and interconnect networks 1080, configuration circuit 1220 and host interface

1240, communicatively coupled as depicted. In accordance with the teachings of the present invention, emulation array and interconnect networks 1080 include dynamically reconfigurable integrated circuits 1200a through 1200n of the present invention, comprising a plurality of LEs 200 which are programmably configured to emulate and "realize" a particular circuit design prior to fabrication of the circuit design. More specifically, innovative dynamically reconfigurable integrated circuits 1200a through 1200n enable a user of the emulation system to control a routing network to selectively output, via a partial scan register, a subset of the state values for select LEs, foregoing the time consuming recompilation process or a full scan output from prior art scan registers typical of prior art emulation systems. Accordingly, emulation systems incorporating the innovative features of the present invention, such as emulation system 100, enable a user of such emulation systems to dynamically change visibility points within an emulator without the time consuming process of altering and recompiling the circuit via the design mapping software, a process often measured in days for complex circuit designs.

Reblewski does not disclose the partitions recited in claims 17, 21, 23, and 27.

In figure 3, Reblewski (6473726) discloses a partitioner 134 used in a multiple circuit design system.

In order to facility the emulation if more than one circuit, it would have been obvious to one of ordinary skill in the art for Reblewski (6265894) to incorporate the teachings of Reblewski (6473726).

Relevant Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Agarwal (5596742) discloses an FPGA logic emulation system with interchip connections between the pins where virtual interconnections overcome device pin limitations. A partition of the emulated circuit has a number of interconnections to other partitions.

Sample (6625793) discloses a programmable logic chip used for emulation with a plurality of logic elements, which provides diversity in functionality and interconnections.

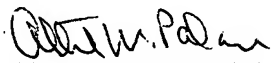
Sample (6377912) discloses an emulation system which reduces hardware costs by providing time multiplexed interconnect signals, thus creating a timed sequence of partitioned emulation circuits.

Quayle (6694464) discloses a hardware emulation system for testing which multiplexes design signals onto a plurality of programmable logic chips. The system includes a processor, RAM, and logic analyzer to analyze the test results for each time dependent configuration.

5. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Albert W. Paladini
Primary Examiner
Art Unit 2125

February 4, 2005